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## **Digital Logic Synthesis and Equivalence Checking Tools ...**

See if this can help you 1. <http://users.ensc>

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.concordia.ca/~tahar/coen7501/notes/lec-slides10.pdf 2. Cadence Encounter Conformal Equivalence Checking User Guide (LEC ...

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## LEQUIVALENCE CHECKER

Cadence Encounter Conformal

Equivalence Checker (EC), ® ® ® makes it possible to verify and debug multi-million-gate designs without using test vectors. It offers the only complete equivalence checking solution available for verifying SoC designs—from RTL to

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final LVS netlist (SPICE)—as well as  
FPGA designs.

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CONFIDENTIAL 1 CADENCE DESIGN  
SYSTEMS, INC.

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Cadence ® Conformal ® Equivalence  
Checker (EC) makes it possible to verify

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and debug multi-million-gate designs without using test vectors. It offers the industry's only complete equivalence checking solution for verifying SoC designs—from RTL to final LVS netlist (SPICE)—as well as FPGA designs.

**CADENCE ENCOUNTER**

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## **CONFORMAL EQUIVALENCE CHECKER DATASHEET ...**

Cadence Conformal suite of tools contains a tool called Logic Equivalence Checker or LEC. Section 4 of this tutorial describes how to formally verify that the synthesized design is functionally equivalent to the RTL description using LEC. This section

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can be skipped if one chooses to use  
Formality for equivalence checking.  
During the ...

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1 The Conformal LEC software does not  
support the `read_comments_as_HDL`

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synthesis directive, and the directive does not affect the Conformal LEC software. Table 17–1 lists supported pragmas and trigger keywords for formal verification. c Do not use Verilog 2001-style pragma declarations. The Quartus II software and the

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## **CONFORMAL LEC TUTORIAL PDF**

### **CONFORMAL LEC TUTORIAL PDF -**

This is a brief introduction on how to using Conformal LEC tool for your IC design. This tutorial provides a quick getting-strated guide to Cadence

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Verification ... CONFORMAL-LEC  
Preferences Window LEC> add compared  
points —all LEC> compare LEC> Compare  
done! Compared points Equi ent Non—equi  
u al ent T -VHDL —Rev i sed

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## **Practical ECOs using Conformal ECO tool - Cadence**

Gates On the Fly Use Case: Conformal  
LEC failures debug [www.nandigits.com](http://www.nandigits.com)  
Conformal LEC schematic Conformal  
LEC GUI debug tool gave some useful  
information, but not sufficient and



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efficient. The schematic from LEC debug tool printed out too many gates and connections. The culprit gates were hiding somewhere.

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**Conformal ECO Steps R1 vs R2 •**

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Compare LEC golden RTL and Modified RTL. • Review the non-equivalence points. R1 vs LAY1 • Compare Golden PNR netlist with original RTL. This should be clean. R2 vs G2 • New RTL with ECO fix compared with synthesized netlist of R2 for equivalence. This should be clean. LAY1 vs G2 • Non-equivalence

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expected.

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Computer-Aided VLSI System Design EC  
Lab : Design Verification (Fall, Nov.  
2010) ===== Motivation and Importance  
of Equivalence Checking As a golden  
model is constructed, we prefer to check

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the equivalence between golden model ...  
To understand how to use Conformal LEC  
to formally check the equivalence between  
your VLSI designs in the design ...

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executed in the following order (3.4.0.a or later ): ... User Manual: PDF format file with information related to the product (for example; installation, process flow, and GUI)

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## **Equivalence Checking Using Cadence Conformal LEC**

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Conformal's very own AE team put  
together some cool request, technical  
documentation, solutions and more in your  
personalized. Jan 5, 2019. CADENCE  
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## **17. Cadence Encounter Conformal Support**

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manual.html, 03-Sep-2015 20:15, 9.1K.

(TXT). Encounter/Conformal). The  
SKILL code The generated user interfaces  
guide the engineer through com- pleting



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the greyed out “Insert Scan”, “LEC” and “STA” buttons), but This form

## **Computer-Aided VLSI System Design - ??????**

Best known methods for using Cadence Conformal LEC at Intel 3 The design that we use as our test case is a high-

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performance, dual-port gigabit Ethernet controller for servers and embedded system design [7].

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3. User -manual-cadence Design Systems-  
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In this paper we will explore how to use  
the Cadence Conformal LEC tool  
capabilities to verify different types of  
designs, based on the.

**Conformal Equivalence Checker -**

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## **Cadence Design Systems**

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Conformal ® LEC Logic Equivalence

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