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AEE Appendix C.2 16.(page  
C16) 1. solution point 2.  
graph 3. Algebraic, graphical,  
numerical 4. 1.If possible,  
rewrite the equation so that  
one of the variables is  
isolated on one side of the**

**equation. 2. Make a table of values showing several solution points. 3. Plot these points on a rectangular coordinate system. 4.**

## **Appendix C The Basics of Logic Design**

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Pipelining Reference:  
Appendix C, Hennessy &  
Patterson ... | This is the  
solution shown in Figure C11 |  
The branch penalty is fixed and  
cannot be reduced by**

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B.1 question is L1 cache ,the  
latencies (in CPU cycles) of  
different kinds of access are  
follows: cache hit , 1 cycle**

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**;cache miss,105 cycle; main  
memory access with cache  
disable ,100 cycles a.) when  
you run a program with an  
overall miss rate of 5% what  
will the avg. memory ...**

**Elsevier: Hennessy,**

*Page 16/44*



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4th edition (September 13,  
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**Digital electronics operate with only two voltage levels of interest: a high voltage and a low voltage. ... C-6**

**Appendix C The Basics of Logic Design. Logic Equations Show the logic equations for the logic functions, D, E, and**

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**F, described in the previous example.**

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**truth table representation of a logic function are equivalent. (We discuss this in further detail in Appendix C.) However, when a**

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